4-Channel LDO PMIC for Camera Applications

DESCRIPTION

The CNS2866 is a 4-Ch LDO PMIC for camera sensor applications, which include 2-Ch DVDD, 2-Ch AVDD.

CNS2866 used N-MOSFET architecture for DVDD LDOs. Ultra-low dropout voltage (Typ.80mV @ 0.5A Load) of DVDD LDOs is designed for high efficiency and lower power dissipation purpose.

CNS2866 used P-MOSFET architecture for AVDD LDOs. Ultra-high PSRR and ultra-low output noise are designed for noise sensitive camera application.

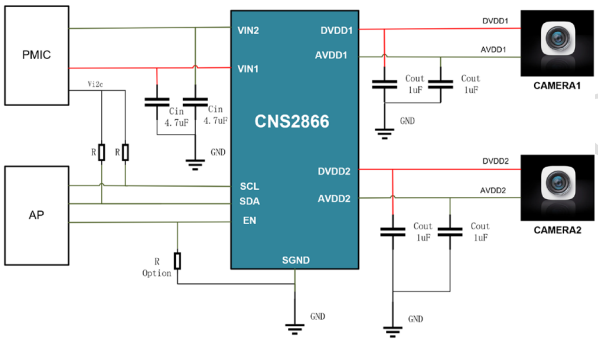
With the highly integrate and small package size design, CNS2866 is available in DFN2x2-10L package.

FEATURES

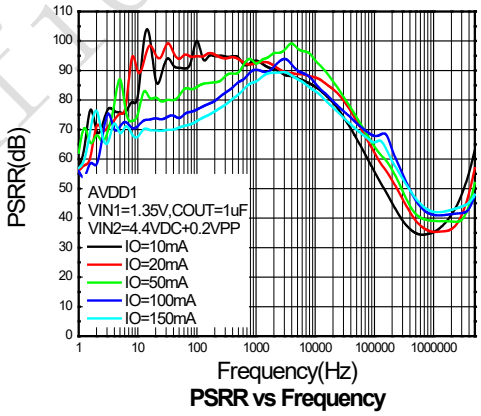
- Flexible function setting by I2C @ 400K Hz
- VIN2 Input UVLO
- Over temperature protection
- Over current protection
- Soft start function
- DVDD1/2 dropout voltage: 80mV@0.5A
- DVDD1/2 output current: 820mA Min.
- AVDD1/2 output current: 300mA Min.
- AVDD LDO PSRR:90dB
- AVDD LDO output noise:8uV
- Pb-free and halogen-free.

APPLICATIONS

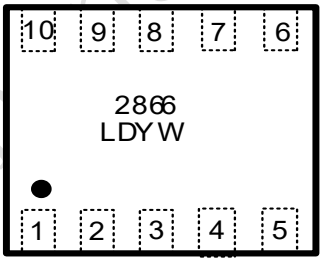
- Smartphones
- AR/XR
- IP Camera



Typical application



AVDD LDO PSRR



Marking

2866 : Device Code

LD : Special Code

Y : Year Code

W : Week Code

Order Information

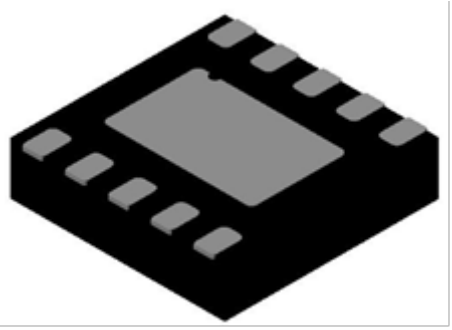
Device	Package	Shipping
CNS2866-10/TR	DFN2x2-10L	3000/Reel&Tape

目录

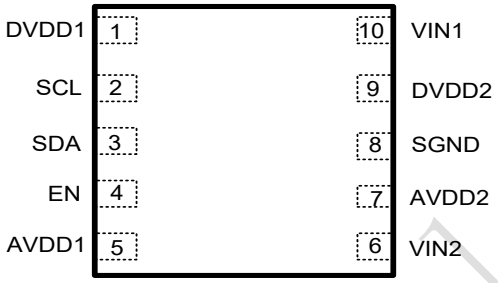
DISCLAIMER

CHANALOG reserves the right to make any change in circuit design, or specifications without prior notice.

1 Pin configuration



DFN2x2-10L (Bottom View)



Pin configuration (Top view)

2 Pin description

Pin No.	NAME	DESCRIPTION
1	DVDD1	LDO1 output
2	SCL	I2C interface
3	SDA	
4	EN	Global enable control, Active high. Maintain to low if I2C control used
5	AVDD1	LDO3 output
6	VIN2	LDO3~LDO4 Supply input, LDO1, LDO2 bias
7	AVDD2	LDO4 output
8	SGND	Ground
9	DVDD2	LDO2 output
10	VIN1	LDO1, LDO2 supply input
exposed pad	-	The exposed pad should be connected to a large ground plane to maximize thermal performance.

3 Specifications

3.1 Absolute Maximum Ratings (1) (2)

Parameter		Value	Unit
V_{IN} Range (VIN1, VIN2)		-0.3~6.5	V
V_{EN} Range		−0.3 to V_{IN} + 0.3	V
V_{OUT} Range		−0.3 to V_{IN} + 0.3	V
I_{OUT}		Check EC table	mA
Lead Temperature Range		260	ºC
Storage Temperature Range		-55 ~ 150	ºC
Operating Junction Temperature Range		150	ºC
MSL		Level-3	
ESD Ratings	HBM	Class-2	V
	MM	300	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and the device is not switching. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

3.2 Recommended Operating Conditions

Parameter	Value	Unit
VIN1 Operating Supply Voltage Range	0.6~2.0	V
VIN2 Operating Supply Voltage Range	3~5.5	V
Operating Temperature Range	-40～85	ºC

3.3 Thermal Information (3)

THERMAL METRIC		DFN1616	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58	°C/W

(3) Note 1 : Single component mounted on 2 oz, FR 4 PCB with 645 mm2 Cu area

4 Electrical Characteristics

VIN1=1.35V, VIN2=3.3V, CIN=4.7uF, COUT=1uF, Ta = +25°C, unless otherwise noted.

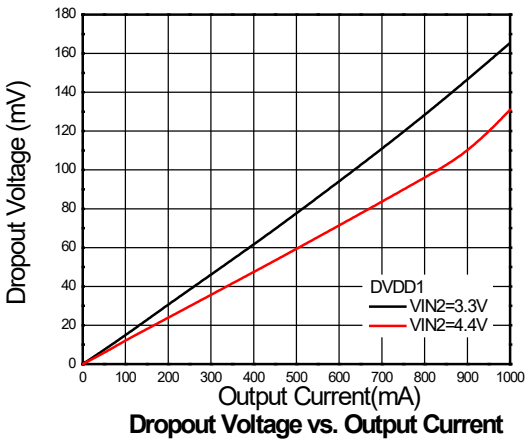
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Whole Device						
Quiescent current at all LDO active	I_Q	EN=H or Enable chip by I2C, No load		65	105	uA
Shutdown current	I_{SHDN}	EN=L or Shutdown by I2C		0.23	1.0	uA
EN logic high voltage	V_{ENH}		1.2			V
EN logic low voltage	V_{ENL}				0.4	V
EN pin leakage current	I_{EN}	VEN= 0 to 5.5V			8	uA
Turn−On Time	T_{ON}	EN=L to H, V_{OUT}=1.2V DVDD1/2 V_{OUT}=V_{OUT} * 90%		0.5		mS
		EN=L to H, V_{OUT}=2.8V, AVDD1/2 V_{OUT}=V_{OUT} * 90%		0.8		mS
Thermal shutdown threshold	T_{SDH}	Iout=1mA		140		ºC
Thermal shutdown hysteresis	$T_{SDH-HYS}$	Iout=1mA		30		ºC
Output discharge resistor ON resistance	R_{DCHG}	EN=L or Shutdown by I2C		400		Ω
Under voltage lock-out	$UVLO_{\_VIN2}$	VIN2 Falling		2.0		V
ULVO hysteresis	$UVLO_{\_HYS}$	VIN2 Rising		0.1		V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
LDO1, LDO2 (DVDDx)						
Input voltage range	VIN1		0.6		2.0	V
Output voltage range	DVDDx		0.6		1.8	V
Default output voltage	DVDDx	EN=H		1.2		V
Output voltage accuracy	V_{OUT_ACC}		-2		+2	%
Output current limit	I_{LIM}	RL=1Ω	820			mA
Short current	I_{SHORT}	V_{OUT}=GND		940		mA
Dropout voltage	V_{DROP}	V_{IN2}=3.3V, V_{OUT}=1.05V, I_{OUT}=500mA		72		mV
		V_{IN2}=3.3V, V_{OUT}=1.2V, I_{OUT}=500mA		80		mV
	V_{DROP}	V_{IN2}=4.4V, V_{OUT}=1.05V, I_{OUT}=500mA		58		mV
		V_{IN2}=4.4V, V_{OUT}=1.2V, I_{OUT}=500mA		60		mV
Load regulation	$\triangle V_{Load}$	V_{IN2}=3.3V, V_{IN1}=1.35V, V_{OUT}=1.2V, I_{OUT}=1~200mA		2		mV
Line regulation	$\triangle V_{LINE}$	V_{IN2}=3.3V, V_{IN1}=1.25~2.0V V_{OUT}=1.2V, I_{OUT}=10mA		0.1		mV
		V_{IN2}=3.0～4.0V, V_{IN1}=1.3V V_{OUT}=1.2V, I_{OUT}=10mA		0.1		mV
Output voltage noise	e_{NO}	V_{IN2}=3.3V, V_{IN1}=1.3V V_{OUT}=1.2V, 10Hz to 100KHz I_{OUT}=0		150		uV
Power Supply Rejection Rate	$PSRR_{\_VIN1}$	V_{IN1}=1.35V+0.2V_{P-P} V_{IN2}=4.4V, V_{OUT}=1.2V I_{OUT}=10mA, F=1KHz, C_{OUT}=1uF		72		dB
	$PSRR_{\_VIN2}$	V_{IN2}=4.4V+0.2V_{P-P} V_{IN1}=1.35V, V_{OUT}=1.2V I_{OUT}=10mA, F=1KHz, C_{OUT}=1uF		45		dB

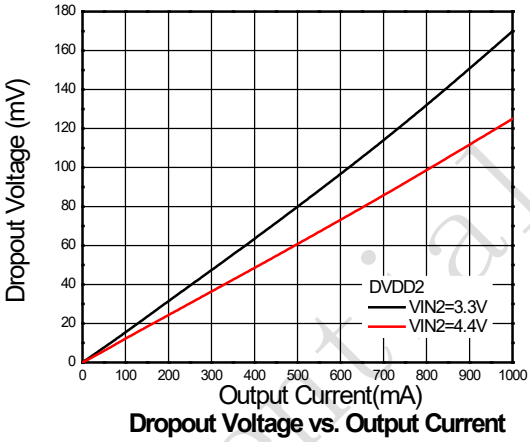
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
LDO3, LDO4 (AVDDx)						
Input voltage range	VIN2		3		5.5	V
Output voltage range	AVDDx		1.2		4.3	V
Default output voltage	AVDDx	EN=H		2.8		V
Output voltage accuracy	V_{OUT_ACC}		-2		+2	%
Output current limit	I_{LIM}	RL=1Ω	300			mA
Short current	I_{SHORT}	V_{OUT}=GND		430		mA
Dropout voltage	V_{DROP}	V_{OUT}=2.8V, I_{OUT}=300mA		90		mV
Load regulation	$\triangle V_{Load}$	V_{IN2}=3.3V, V_{OUT}=2.8V, V_{IN1}=1.35V , I_{OUT}=1~200mA		3		mV
Line regulation	$\triangle V_{LINE}$	V_{IN2}=3.0V~4.0V, V_{OUT}=2.8V, V_{IN1}=1.35V , I_{OUT}=10mA,		0.1		mV
Output voltage noise	e_{NO}	V_{IN2}=3.3V, V_{OUT}=2.8V, V_{IN1}=1.35V , 10Hz to 100KHz I_{OUT}=0		8		uV
Power Supply Rejection Rate	PSRR	V_{IN2}=4.4V+0.2V_{P-P}, V_{IN1}=1.35V, V_{OUT}=2.8V, I_{OUT}=10mA, F=1KHz, C_{OUT}=1uF		92		dB
		V_{IN2}=4.4V+0.2V_{P-P}, V_{IN1}=1.35V, V_{OUT}=2.8V, I_{OUT}=10mA, F=1KHz, C_{OUT}=4.7uF		92		dB
		V_{IN2}=4.4V+0.2V_{P-P}, V_{IN1}=1.35V, V_{OUT}=2.8V, I_{OUT}=10mA, F=1MHz, C_{OUT}=1uF		35		dB
		V_{IN2}=4.4V+0.2V_{P-P}, V_{IN1}=1.35V, V_{OUT}=2.8V, I_{OUT}=10mA, F=1MHz, C_{OUT}=4.7uF		48		dB

5 Typical Characteristics

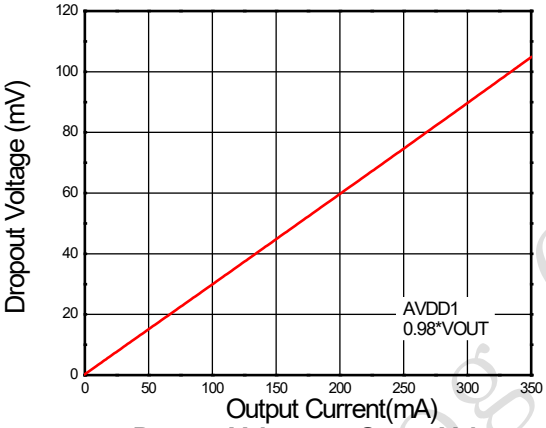
T_A=25°C, C_{IN}=4.7uF, C_{OUT}=1uF , unless otherwise noted



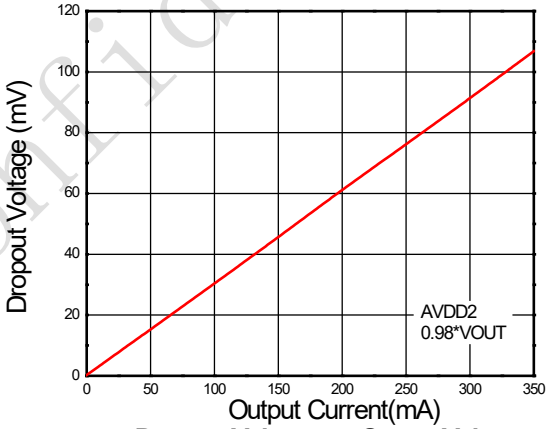
Dropout Voltage vs. Output Current



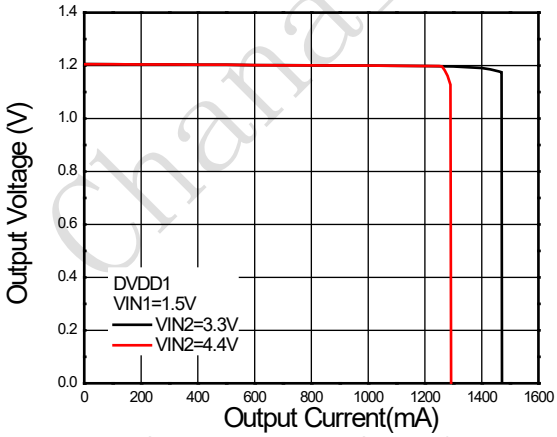
Dropout Voltage vs. Output Current



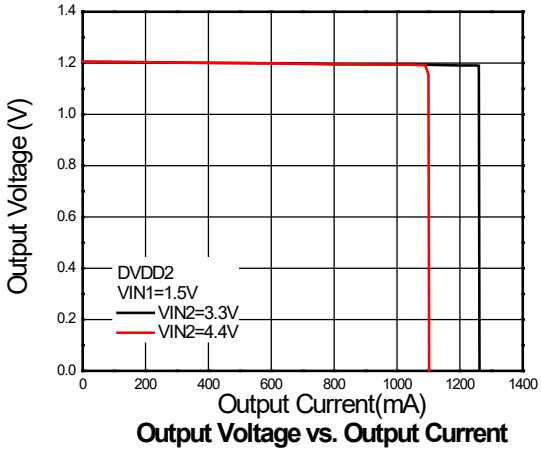
Dropout Voltage vs. Output Voltage



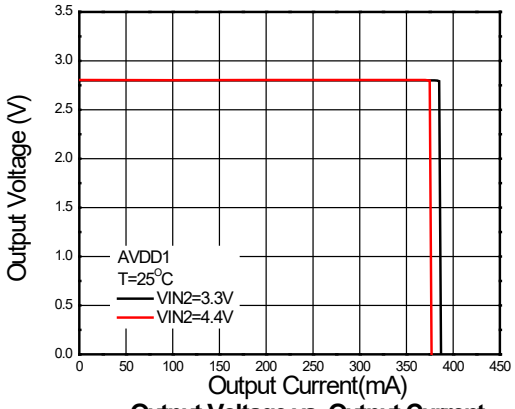
Dropout Voltage vs. Output Voltage



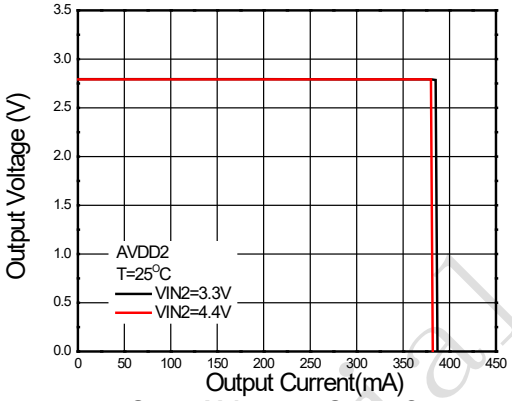
Output Voltage vs. Output Current



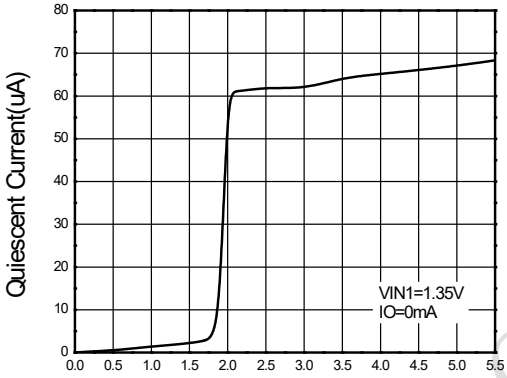
Output Voltage vs. Output Current



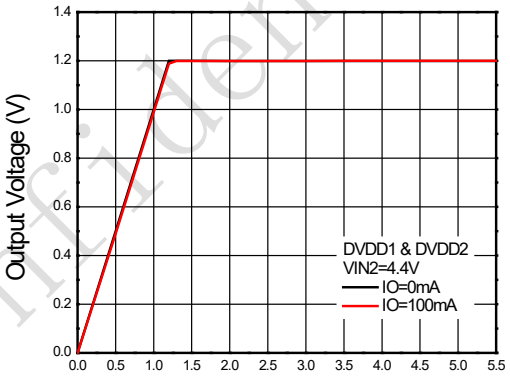
Output Voltage vs. Output Current



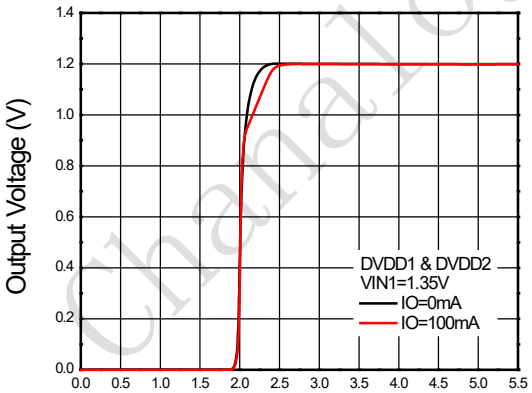
Output Voltage vs. Output Current



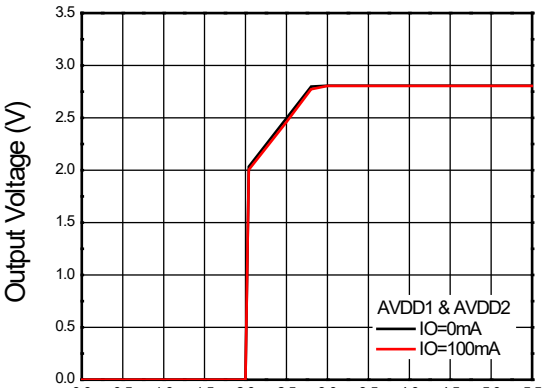
Quiescent Current vs. Input Voltage 2



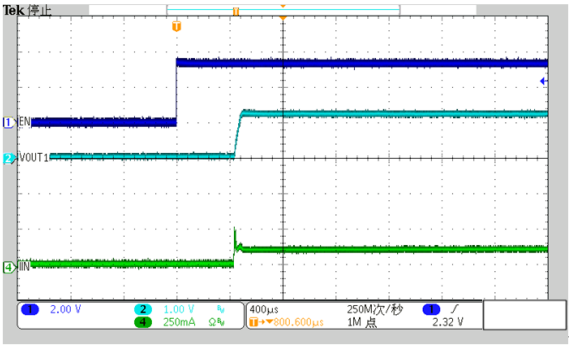
Output Voltage vs. Input Voltage 1



Output Voltage vs. Input Voltage 2

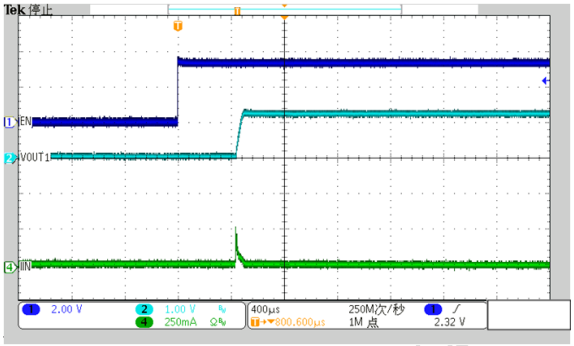


Output Voltage vs. Input Voltage 2



DVDD1 Start up

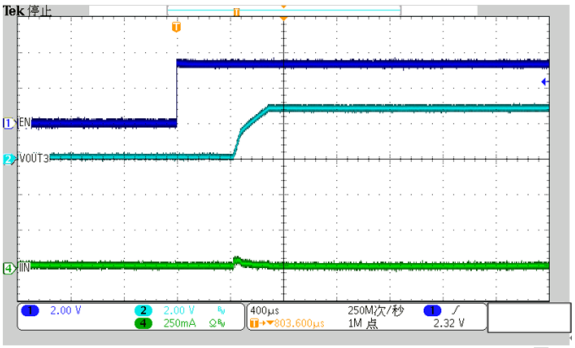
V_{IN1}=1.35V,V_{IN2}=3.3V,I_{OUT}=0mA



DVDD2 Start up

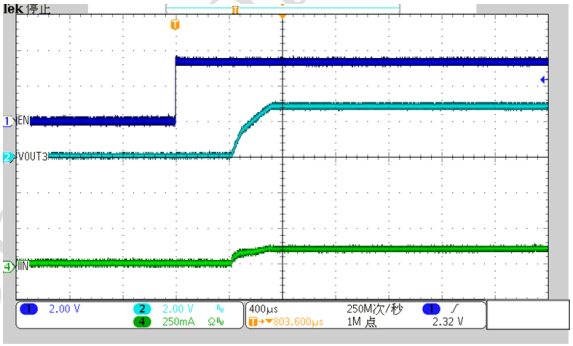
V_{IN1}=1.35V,V_{IN2}=3.3V,I_{OUT}=100mA

AVDD1/2 Start Up



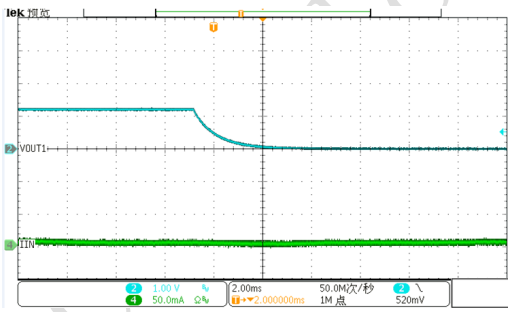
AVDD1 Start up

V_{IN1}=1.35V,V_{IN2}=3.3V,I_{OUT}=0mA



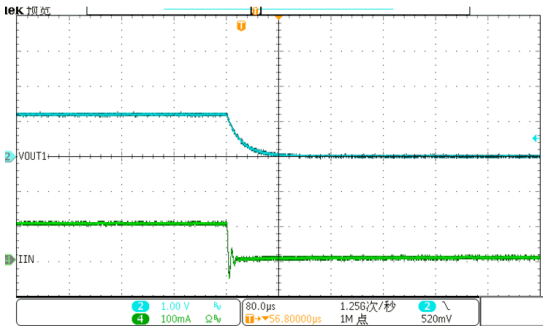
AVDD2 Start up

V_{IN1}=1.35V,V_{IN2}=3.3V,I_{OUT}=100mA



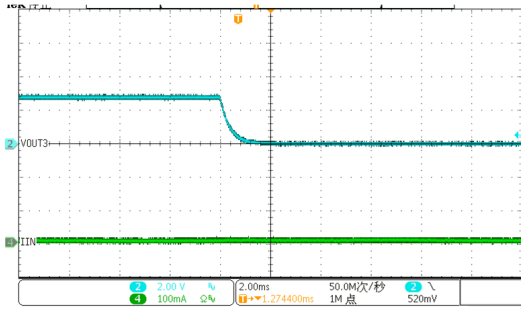
DVDD1 Shut Down

V_{IN1}=1.35V, V_{IN2}=3.3V,I_{OUT}=0mA



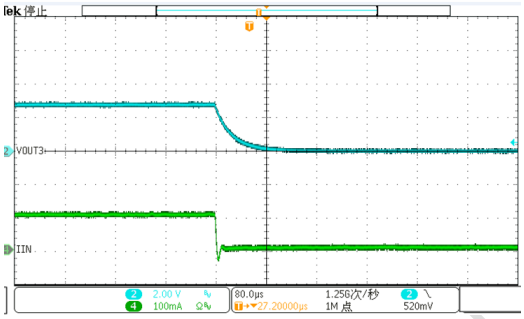
DVDD2 Shut Down

V_{IN1}=1.35V, V_{IN2}=3.3V, I_{OUT}=100mA



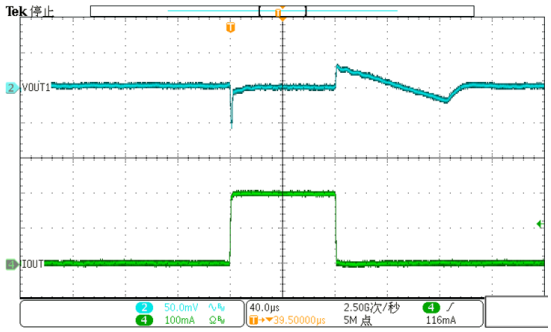
AVDD1 Shut Down

V_{IN1}=1.35V, V_{IN2}=3.3V, I_{OUT}=0mA



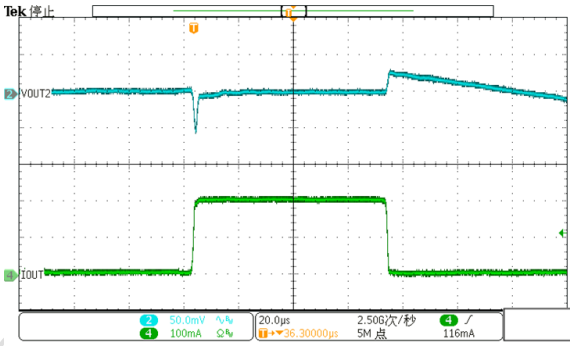
AVDD2 Shut Down

V_{IN1}=1.35V, V_{IN2}=3.3V, I_{OUT}=100mA



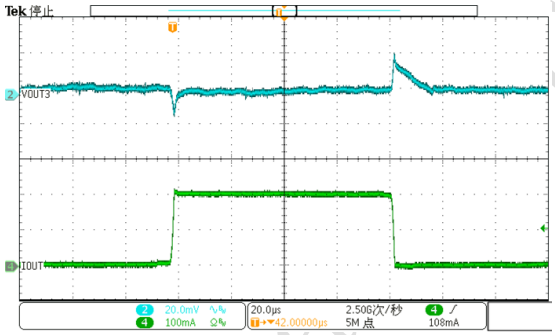
DVDD1, Load Transient

V_{IN1}=1.35V ,V_{IN2}=3.3V,I_{OUT}=1~200mA



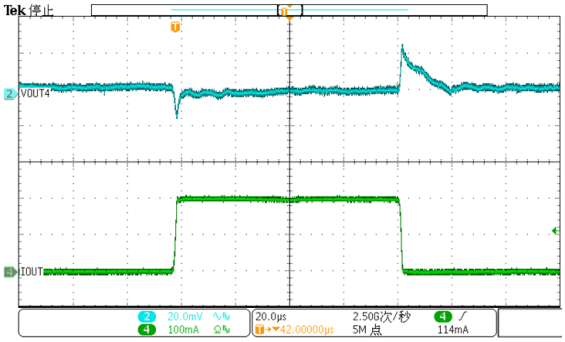
DVDD2, Load Transient

V_{IN1}=1.35V ,V_{IN2}=3.3V,I_{OUT}=1~200mA



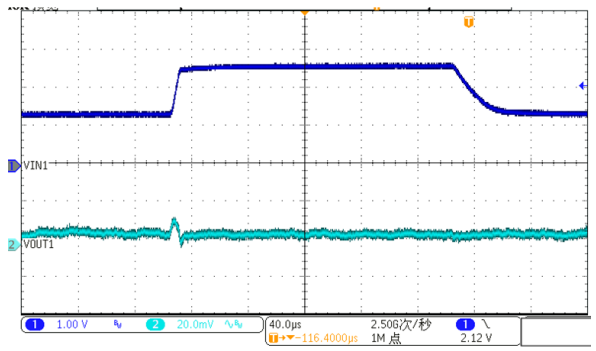
AVDD1, Load Transient

V_{IN2}=3.3V,I_{OUT}=1~200mA



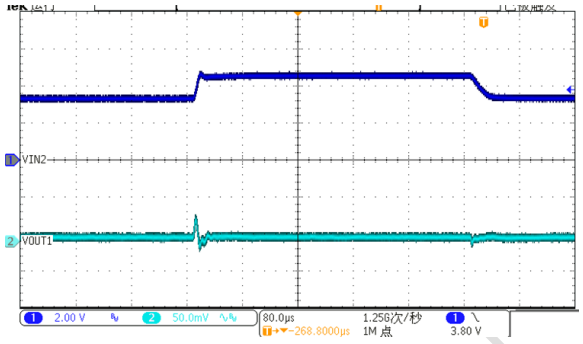
AVDD2, Load Transient

V_{IN2}=3.3V,I_{OUT}=1~200mA



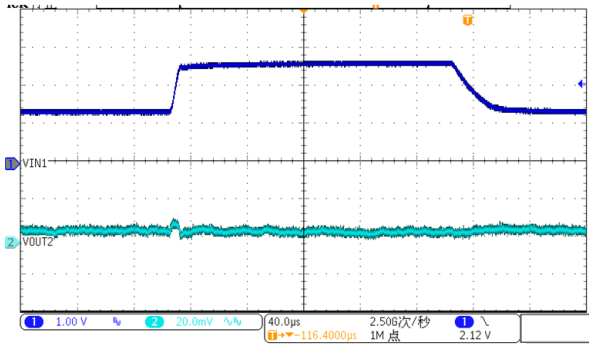
DVDD1 Line Transient

VIN1=1.3~2.6V, VIN2=3.3V, IOUT=1mA



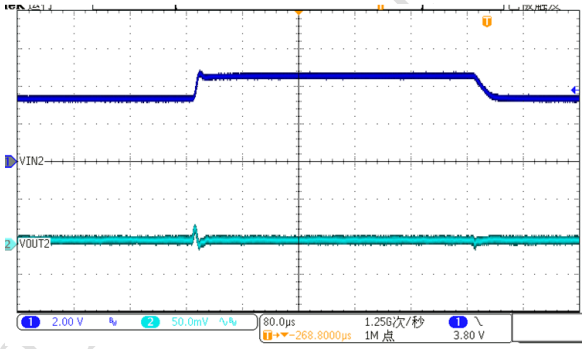
DVDD1 Line Transient

VIN1=1.35V, VIN2=3.3~4.5V, IOUT=1mA



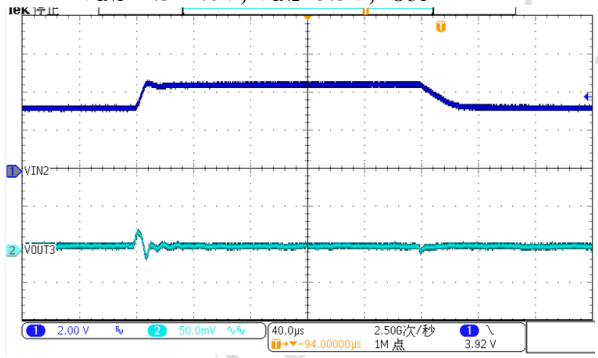
DVDD2 Line Transient

V_{IN1}=1.3~2.6V, V_{IN2}=3.3V, I_{OUT}=1mA



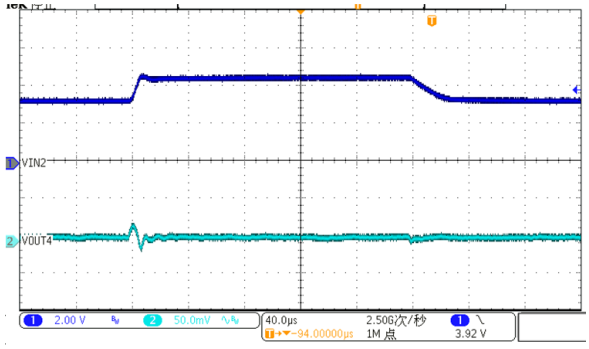
DVDD2 Line Transient

V_{IN1}=1.35V, V_{IN2}=3.3~4.5V, I_{OUT}=1mA



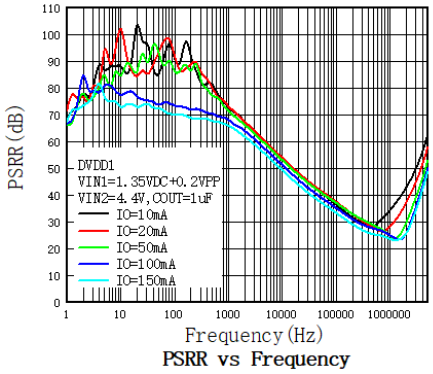
AVDD1 **Line Transient**

VIN2=3.3-4.5V, IOUT=1mA

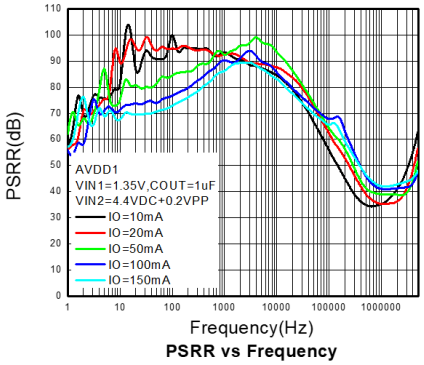


AVDD2 **Line Transient**

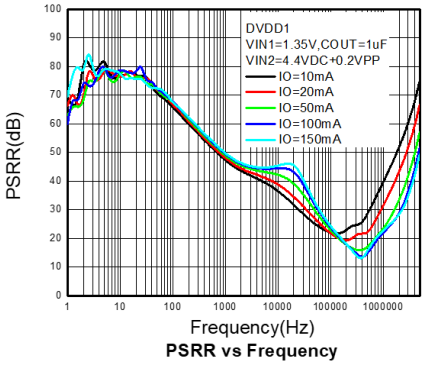
VIN2=3.3~4.5V, IOUT=1mA



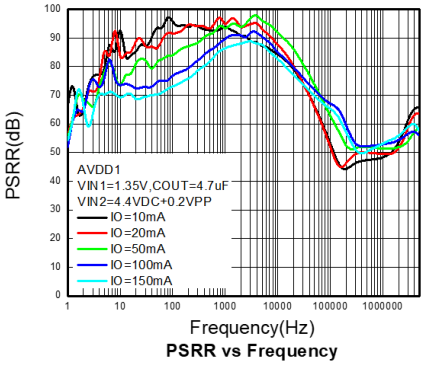
PSRR vs Frequency



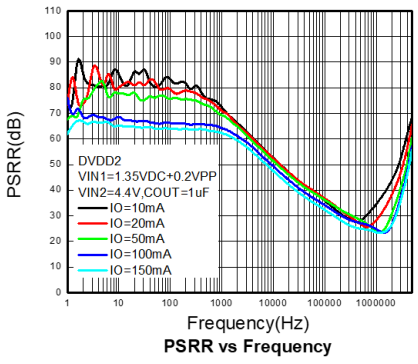
PSRR vs Frequency



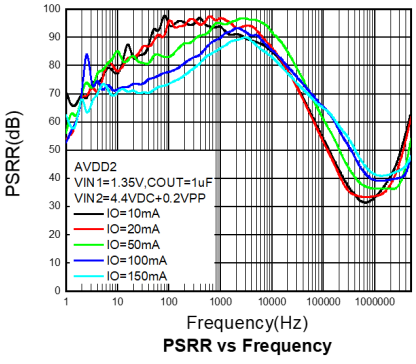
PSRR vs Frequency



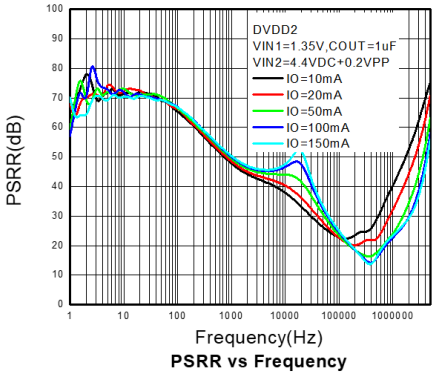
PSRR vs Frequency



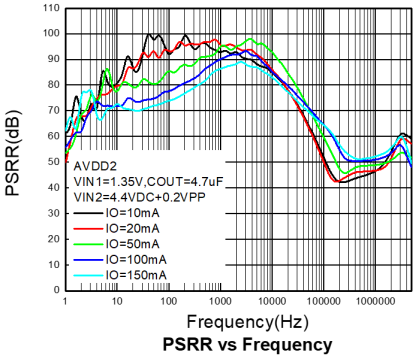
PSRR vs Frequency



PSRR vs Frequency



PSRR vs Frequency

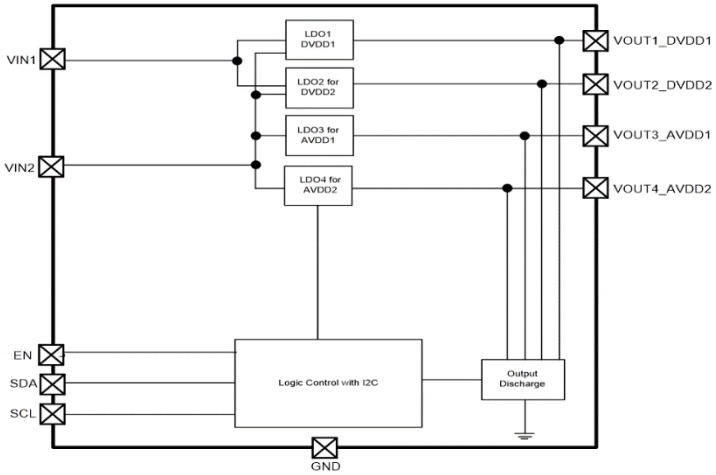


PSRR vs Frequency

6 Detail description

6.1 Overview

The CNS2866 is a 4-Ch LDO PMIC for camera sensor applications, which include 2-Ch DVDD, 2-Ch AVDD. CNS2866 used N-MOSFET architecture for DVDD LDOs. Ultra-low dropout voltage (Typ.80mV @ 0.5A Load) of DVDD LDOs is designed for high efficiency and lower power dissipation purpose. CNS2866 used P-MOSFET architecture for AVDD LDOs with Ultra-high PSRR and ultra-low output noise for camera application. CNS2866 has integrated a standard 400K Hz I2C slave device. The function setting is flexible such as power sequence, output voltage, output discharge through I2C. The chip enable control support EN pin control and I2C control. For more details, please refer to the Functional block diagrams as follows:



6.2 Feature description

6.2.1 Power up/down control

CNS2866 has 4 LDO regulators. Power up/down of each regulator can be controlled by the following three ways. It can be set at the registers $DVDD_X$_SEQ[3:0] & $AVDD_X$_SEQ[3:0] (x=1 to 4) respectively.

A. External EN pin toggles from low to high, it will force $DVDD_X$ & $AVDD_X$ regulators powered up.
B. Individual on/off control.
C. Automatic power up/down sequence control.

A. Chip enable control

External EN pin toggles from low to high, it will force $DVDD_X$ & $AVDD_X$ regulators powered up, output voltage of each LDO is default voltage, check EC Table. When external EN pin is low, LDO output can be controlled by an I2C register.

B. Individual on/off control.

Power-up and shut down of each regulator can be controlled by an I2C register. $DVDD_X$_EN &AVDDX_EN are internal signals to enable one of regulators, If $DVDD_X$_SEQ[3:0] & $AVDD_X$_SEQ[3:0] set to '0000', that $DVDD_X$ & $AVDD_X$ channels can be controlled directly by a bit specified in register $DVDD_X$_EN &AVDDX_EN .

$DVDD_X$_VOUT[7:0] & $AVDD_X$_VOUT[7:0] can set output voltage of each channel.

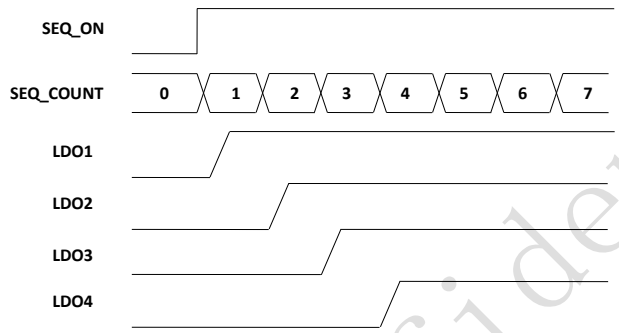
C. Automatic power up/down sequence control.

CNS2866 has seven SLOTs to which each regulator can be assigned.

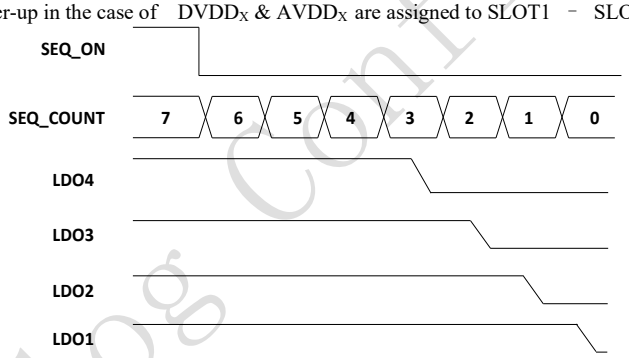
SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	SLOT7

They are started by SEQ_ON signal. when SEQ_ON is high. Internal counter SEQ_COUNT[2:0] starts increments from 0 (“000”) to 7 (“111”). When SEQ_ON is low, SEQ_COUNT[2:0] decrements from 7 (“111”) to 0 (“000”). Regulators assigned to one of SLOTs starts power-up or power-down when SEQ_COUNT[2:0] matches the SLOT number.

Internal logic signal SEQ_ON is asserted by I2C, write ‘00’ to SEQ_CTRL[1:0] will set SEQ_ON to ‘0’, while write ‘01’ to SEQ_CTRL[1:0] will set SEQ_ON to ‘1’.



Example of Power-up in the case of $DVDD_X$ & $AVDD_X$ are assigned to SLOT1 – SLOT4 respectively



Example of Shutdown in the case of $DVDD_X$ & $AVDD_X$ are assigned to SLOT1 – SLOT4 respectively.

6.2.2 Output discharge

An internal pulldown MOSFET connects a resistor from OUT to ground when the device is disabled to actively discharge the output capacitance. Set related bits to select output discharge function for Discharge Resistor (0x02H Register): 0 is Disable, 1 is Enable.

6.2.3 Under Voltage Lockout

To avoid mis-operation of the device at low input voltages, under voltage lockout is implemented that shuts down the device while VIN2 voltages lower than $UVLO_{VIN2}$.

6.2.4 Soft Startup

After enabling the device, internal soft startup circuitry in CNS2866 ramps up the output to target voltage in startup time. This avoids excessive inrush current and creates a smooth output voltage rise slope.

6.2.5 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick wall scheme. In a high-load current fault or output short events, the brick wall scheme limits the output current to the current limit. When a current limit event occurs, the

device begins to heat up because of the increase in power dissipation. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown.

6.2.6 Thermal Shutdown

The device enters thermal shutdown once the junction temperature exceeds the thermal shutdown rising threshold T_{SDH}. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

6.2.7 I2C interface

CNS2866 utilizes I2C interface to write / read internal registers. It supports 100Kbps standard mode 400Kbps fast mode.

I2C Serial Data Bus

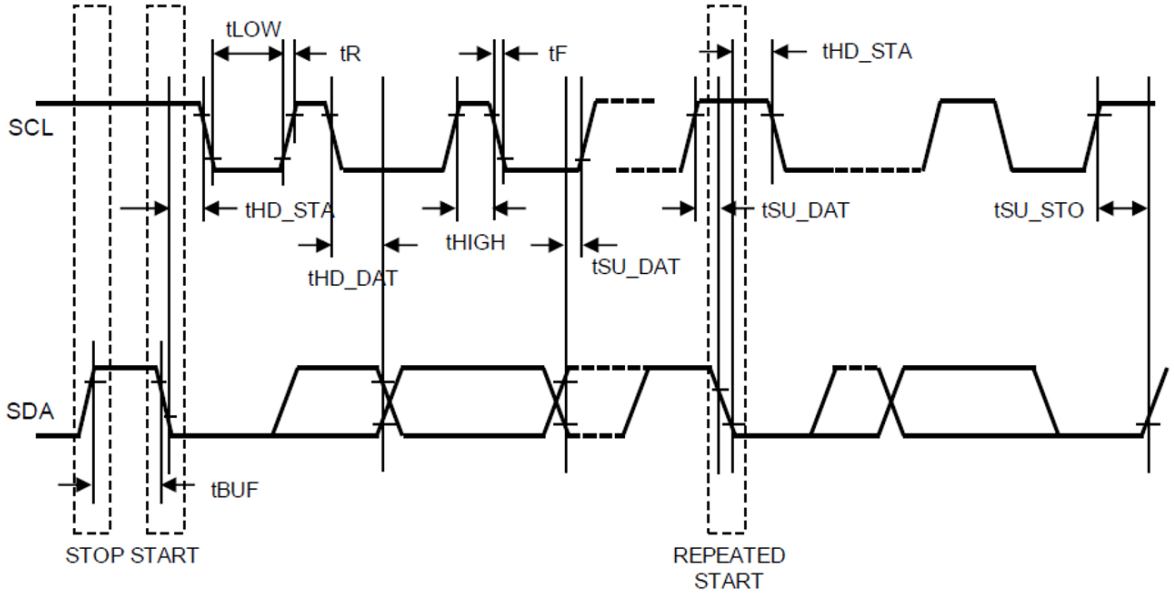


Figure 1, I²C mode timing

The CNS2866 supports the I2C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the bus is called a master, whereas the devices controlled by the master are known as slaves. A master device must generate the serial clock (SCL), control bus access and generate START and STOP conditions to control the bus. The CNS2866 operates as a slave on the I2C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The CNS2866 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The following bus protocol has been defined (Figure 1 and Figure 2). Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy

Both data and clock lines remain HIGH.

Start Data Transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

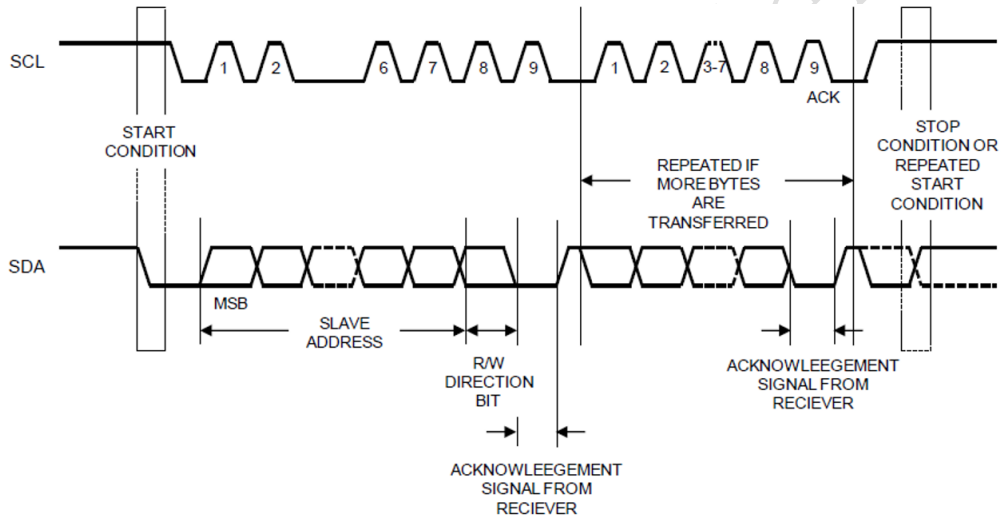


Figure2, Data transfer on I^2C bus

Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2. **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The CNS2866 can operate in the following two modes:

1. **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 3 for Interface). The slave address byte is the first byte received after the

master generates the START condition. The slave address byte contains the CNS2866 address followed by the direction bit (R/W), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the CNS2866 acknowledges the slave address + write bit, the master transmits a register address to the CNS2866. This sets the register pointer on the CNS2866. The master may then transmit zero or more bytes of data, with the CNS2866 acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.

2. Slave Transmitter Mode (Read Mode): The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the CNS2866 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the CNS2866 address followed by the direction bit (R/W), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The CNS2866 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The CNS2866 must receive a "not acknowledge" to end a read.

The 7-bit slave device address is 0101 000 binary

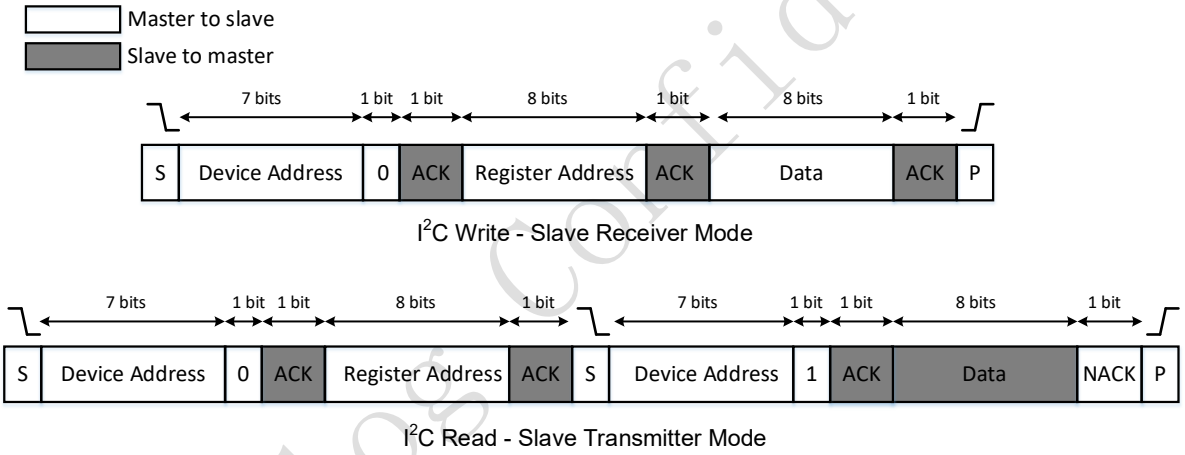


Figure 3, I²C Read/Write operation

Where

S	= START condition
P	= STOP condition
Device Address	= 0101 000 (7 bits, MSB first)
Register Address	= Reg0 – Reg15 address (8 bits)
Data	= data to read or write (8 bits)
1	= Read command bit
0	= Write command bit
ACK	= acknowledge (SDA low)
NACK	= not acknowledge (SDA high)

6.3 Register Description

6.3.1 Global register mapping

Add	Name	Read/ Write	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	Chip_REV	R	0x00	Chip_REV[7:0]							
0x01	N.A.	RW	0x00	N.A.							
0x02	DISCR	RW	0x00					Discharge Resistor Enable/Disable			
0x03	DVDD1_VOUT	RW	0x64	DVDD1_VOUT[7:0]							
0x04	DVDD2_VOUT	RW	0x64	DVDD2_VOUT[7:0]							
0x05	AVDD1_VOUT	RW	0x80	AVDD1_VOUT[7:0]							
0x06	AVDD2_VOUT	RW	0x80	AVDD2_VOUT[7:0]							
0x07	N.A.	RW	0x00	N.A.							
0x08	N.A.	RW	0x00	N.A.							
0x09	N.A.	RW	0x00	N.A.							
0x0A	DVDD1/2_SEQ	RW	0x00	DVDD2_SEQ[3:0]				DVDD1_SEQ[3:0]			
0x0B	AVDD1/2_SEQ	RW	0x00	AVDD2_SEQ[3:0]				AVDD1_SEQ[3:0]			
0x0C	N.A.	RW	0x00	N.A.							
0x0D	N.A.	RW	0x00	N.A.							
0x0E	ENCR	RW	0x00	N.A.				AVDD2_ EN	AVDD1_ EN	DVDD2 _EN	DVDD1_ EN
0x0F	SEQCR	RW(bit4~7) R(bit3~0)	0x00	SEQ_SPEED[1:0]		SEQ_CTRL[1:0]		SEQ_ON	SEQ_COUNT[2:0]		

6.3.2 Register detail description

Chip_REV, Device ID register (0x00)

Add	Name	Read/ Write	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	Chip_REV	R	0x00	Chip_REV[7:0]							

Indicates the device ID with revision. Read only.

DISCR, Discharge Resistor control register (0x02)

Add	Name	Read/ Write	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	DISCR	RW	0x00					Discharge Resistor Enable/Disable			

Each LDO regulators output discharge resistor enable control.

Bit0 for DVDD1, Bit1 for DVDD2,

Bit2 for AVDD1, Bit3 for AVDD2.

0= Disable, 1= Enable

*Note: When use the Discharge Function, should set Bit7 =1.

DVDD1_VOUT[7:0] & DVDD2_VOUT[7:0], DVDDx output voltage setting register (0x03,0x04)

Add	Name	Read/ Write	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	DVDD1_VOUT	RW	0x64	DVDD1_VOUT[7:0]							
0x04	DVDD2_VOUT	RW	0x64	DVDD2_VOUT[7:0]							

Define the Output Voltage Level of DVDD1 & DVDD2

$VOUT_X = 0.6V + DVDD_X\_VOUT[7:0] * 0.006V$

The following table shows the code of each voltage setting for reference

Dec.	Binary	Hex.	Voltage (V)	Dec.	Binary	Hex.	Voltage (V)
0	0000 0000	00H	0.6000	85	0101 0101	55H	1.11
	******			86	0101 0110	56H	1.116
60	0011 1100	3CH	0.96	87	0101 0111	57H	1.122
61	0011 1101	3DH	0.966	88	0101 1000	58H	1.128
62	0011 1110	3EH	0.972	89	0101 1001	59H	1.134
63	0011 1111	3FH	0.978	90	0101 1010	5AH	1.14
64	0100 0000	40H	0.984	91	0101 1011	5BH	1.146
65	0100 0001	41H	0.99	92	0101 1100	5CH	1.152
66	0100 0010	42H	0.996	93	0101 1101	5DH	1.158
67	0100 0011	43H	1.002	94	0101 1110	5EH	1.164
68	0100 0100	44H	1.008	95	0101 1111	5FH	1.17
69	0100 0101	45H	1.014	96	0110 0000	60H	1.176
70	0100 0110	46H	1.02	97	0110 0001	61H	1.182
71	0100 0111	47H	1.026	98	0110 0010	62H	1.188
72	0100 1000	48H	1.032	99	0110 0011	63H	1.194
73	0100 1001	49H	1.038	100	**0110 0100**	**64H**	**1.20**
74	0100 1010	4AH	1.044	101	0110 0101	65H	1.206
75	0100 1011	4BH	1.05	102	0110 0110	66H	1.212
76	0100 1100	4CH	1.056	103	0110 0111	67H	1.218
77	0100 1101	4DH	1.062	104	0110 1000	68H	1.224
78	0100 1110	4EH	1.068	105	0110 1001	69H	1.23
79	0100 1111	4FH	1.074	106	0110 1010	6AH	1.236
80	0101 0000	50H	1.08	107	0110 1011	6BH	1.242
81	0101 0001	51H	1.086	108	0110 1100	6CH	1.248
82	0101 0010	52H	1.092	109	0110 1101	6DH	1.254
83	0101 0011	53H	1.098	110	0110 1110	6EH	1.26
84	0101 0100	54H	1.104	~255	******		

AVDD1_VOUT[7:0] & AVDD2_VOUT[7:0] AVDDx output voltage setting register (0x05,0x06)

Add	Name	Read/ Write	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x05	AVDD1_VOUT	RW	0x80	AVDD1_VOUT[7:0]							
0x06	AVDD2_VOUT	RW	0x80	AVDD2_VOUT[7:0]							

Define the Output Voltage Level of AVDD1& AVDD2

$VOUT_X = 1.2V + AVDD_X\_VOUT[7:0] * 0.0125V.$

The following table shows the code of each voltage setting for reference

Dec.	Binary	Hex.	Voltage (V)	Dec.	Binary	Hex.	Voltage (V)
0	0000 0000	00H	1.2000	**128**	**1000 0000**	**80H**	**2.8000**
1	0000 0001	01H	1.2125	129	1000 0001	81H	2.8125
2	0000 0010	02H	1.2250	130	1000 0010	82H	2.8250
3	0000 0011	03H	1.2375	131	1000 0011	83H	2.8375
4	0000 0100	04H	1.2500	132	1000 0100	84H	2.8500
5	0000 0101	05H	1.2625	133	1000 0101	85H	2.8625
6	0000 0110	06H	1.2750	134	1000 0110	86H	2.8750
7	0000 0111	07H	1.2875	135	1000 0111	87H	2.8875
8	0000 1000	08H	1.3000	136	1000 1000	88H	2.9000
9	0000 1001	09H	1.3125	137	1000 1001	89H	2.9125
10	0000 1010	0AH	1.3250	138	1000 1010	8AH	2.9250
11	0000 1011	0BH	1.3375	139	1000 1011	8BH	2.9375
12~127	******			~255	******		

DVDD1/2_SEQ & AVDD1/2_SEQ: Sequence setting register (0x0A,0x0B)

Add	Name	Read/ Write	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0A	DVDD1/2_ SEQ	RW	0x00	DVDD2_SEQ[3:0]				DVDD1_SEQ[3:0]			
0x0B	AVDD1/2_ SEQ	RW	0x00	AVDD2_SEQ[3:0]				AVDD1_SEQ[3:0]			

Power sequence setting register. there are 7 time slots defined as following table. The power-up sequence is start from slot1 to slot7, and shut down start from slot7 to slot1. Power-up and shut down of each LDO regulator can be set at any one of the slots.

Register Value	Slot Setting
4b'0000	Controlled by register ENCR (0x0E)
4b'x001	Slot1
4b'x010	Slot2
4b'x011	Slot3
4b'x100	Slot4
4b'x101	Slot5
4b'x110	Slot6
4b'x111	Slot7

In the case of that register value of $DVDD_X$_SEQ[3:0] & $AVDD_X$_SEQ[3:0] ,are set to be default "0000", that $DVDD_X$ and $AVDD_X$ regulators will be controlled by register ENCR (0x0E).

ENCR Individual control register (0x0E)

Add	Name	Read/ Write	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0E	ENCR	RW	0x00	N.A.				AVDD2 _EN	AVDD1 _EN	DVDD2 _EN	DVDD1 _EN

Chip enable control register by I2C while the register value of $DVDD_X$_SEQ[3:0] & $AVDD_X$_SEQ[3:0] are set to be default "0000". This register can be written to enable or disable the corresponding LDO regulator. Bit0 for DVDD1_EN, Bit1 for DVDD2_EN, Bit2 for AVDD1_EN, Bit3 for AVDD2_EN. 0: disable, 1: enable.

SEQCR Sequence control register (0x0F)

Add	Name	Read/Write	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0F	SEQCR	RW(bit4~7) R(bit3~0)	0x00	SEQ_SPEED[1:0]		SEQ_CTRL [1:0]		SEQ_ON	SEQ_COUNT[2:0]		

SEQ_SPEED[1:0] define the slot period as following:

Register Value	Slot period(ms)
2b'00	2.00
2b'01	1.00
2b'10	0.50
2b'11	0.25

SEQ_CTRL[1:0] enables power-up or shut down of SEQ

Register Value	SEQ Status
2b'x0	Shutdown
2b'x1	Power up

SEQ_ON indicates the activation signal of SEQ, read only.

Register Value	SEQ Status
1b'0	Shutdown
1b'1	Power up

SEQ_COUNT[2:0] indicates the slot number of SEQ at the moment. Read only.

Register Value	Slot Setting
3b'000	No LDO starts
3b'001	Slot1 starts
3b'010	Slot2 starts
3b'011	Slot3 starts

3b'100	Slot4 starts
3b'101	Slot5 starts
3b'110	Slot6 starts
3b'111	Slot7 starts and stop counting

7 Application and implementation

NOTE

Information in the following applications sections is not part of the CHANALOG component specification, and CHANALOG does not warrant its accuracy or completeness. CHANALOG's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality and stability.

7.1 Application information

The following section discusses the application design of CNS2866, figure 4 shows the typical application circuit for the CNS2866.

7.2 Typical application

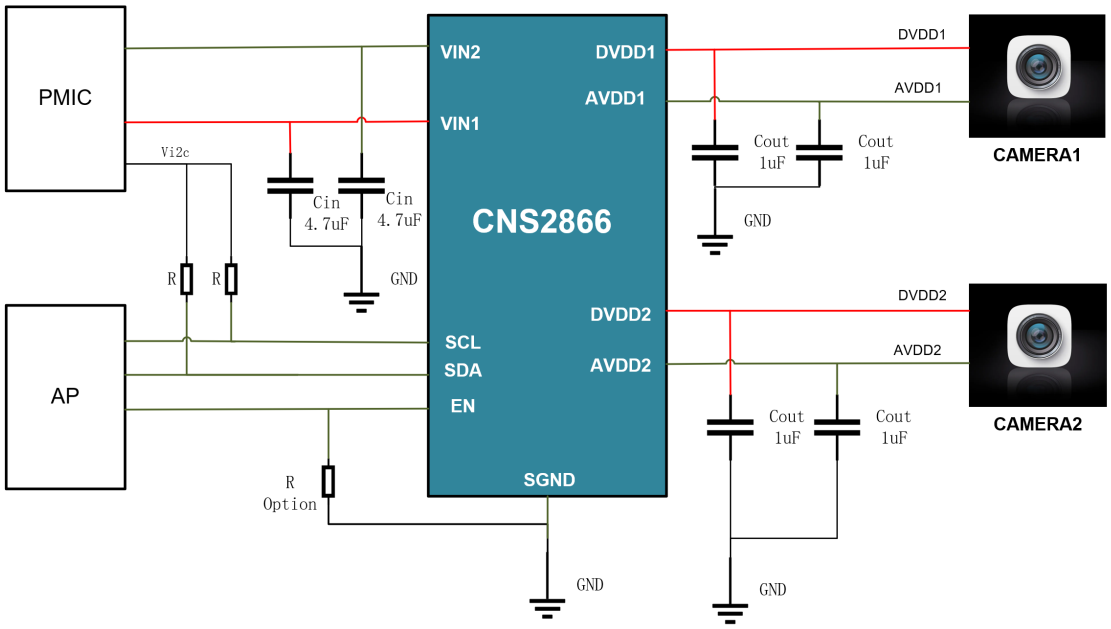


Figure 4, typical application

Note: If use the 0201 package ceramic capacitors, change Cout to 2.2uf /0201 /6.3V X5R ceramic type.

7.3 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the Recommended Operating Conditions table account for an effective capacitance of approximately 50% of the nominal value.

7.4 Input and Output Capacitor Requirements

The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR, and is recommended if the source impedance is greater than 0.5 ohm. When the source resistance and inductance are sufficiently high, especially in the presence of load transients, the overall system may be susceptible to instability (including ringing and sustained oscillation) and other performance degradation if there is insufficient capacitance between VIN1/VIN2 and GND. A capacitor with a value greater than the minimum may be necessary if large, fast-rise-time load or line transients are anticipated or if the device is located more than a few centimeters from the input power source.

An output capacitor of an appropriate value helps ensure stability and improve dynamic performance.

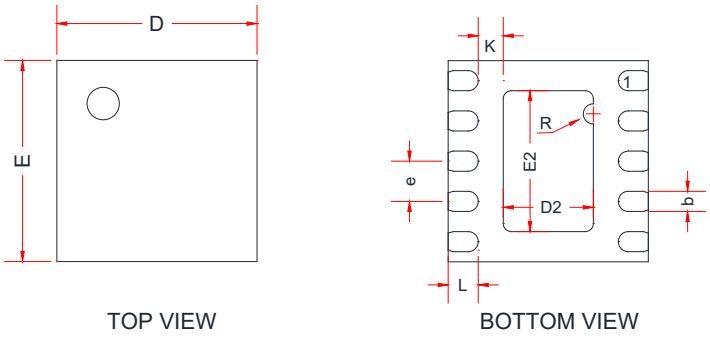
7.5 PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A poor layout design can result in poor line or load regulation and stability issues. For best performance, please follow the below layout guidelines:

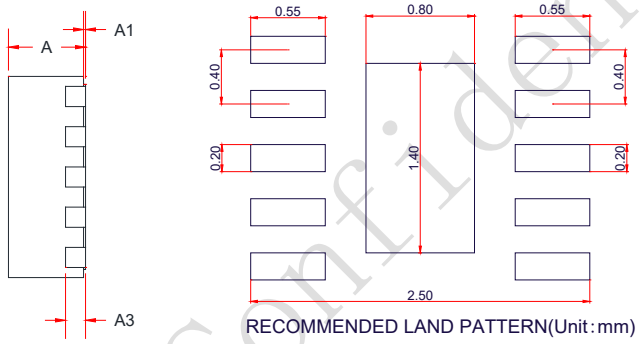
1) Place input and output capacitors as close to the related chip pins as possible, the connection line between capacitors and chip pin should be as short and wide as possible to reduce the noise and EMI interference.
2) Make sure power and ground line wide enough to pass large current.
3) Use copper planes for device connections to optimize thermal performance.The exposed pad of chip must be connected to large area ground layer directly, place sufficient ground vias below the chip to decrease the thermal resistor between chip and PCB.

8 Package information

8.1 Package outline (DFN2x2-10L)



TOP VIEW BOTTOM VIEW

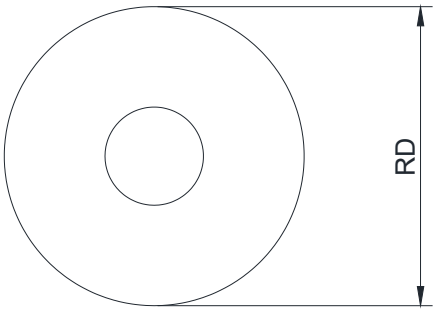


SIDE VIEW RECOMMENDED LAND PATTERN(Unit:mm)

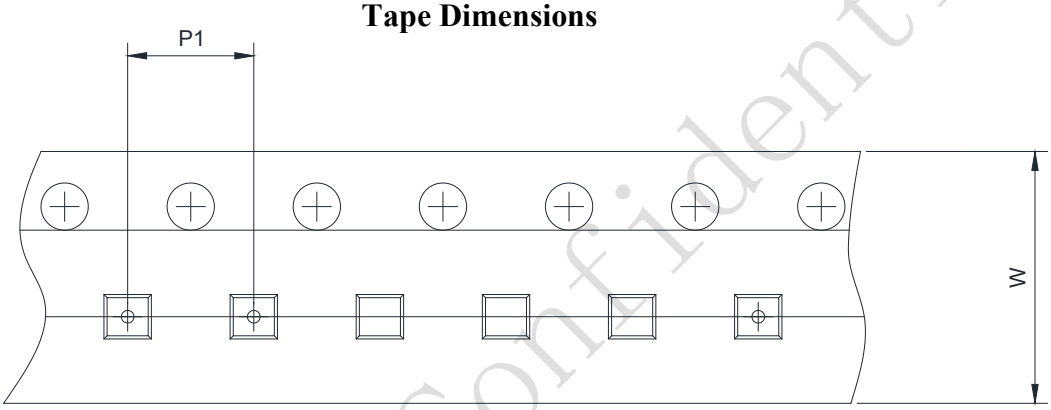
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 Ref.		
b	0.15	0.20	0.25
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.80	0.90	1.00
E2	1.30	1.40	1.50
e	0.30	0.40	0.50
K	0.15	0.25	0.35
L	0.25	0.30	0.35
R	0.10 Ref.		

8.2 Tape and reel information

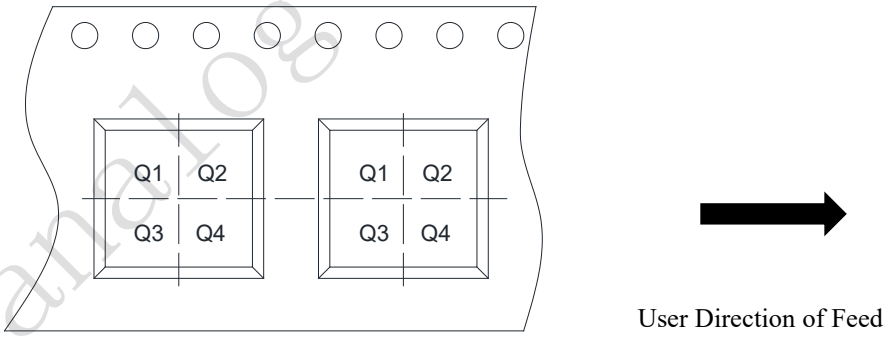
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4